Notice of Allowability	Application No.	Applicant(s)
	10/825,239	HSU ET AL.
	Examiner	Art Unit
	Bryan Bui	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE &amendment filed on 1/25/06*.

2. ☒ The allowed claim(s) is/are *1-22*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Applicants' paper filed on 1/25/2006 has been received and entered. Claims 1, 12, and 18 have been amended. Claims 21 and 22 have been added. Claims 1-22 are pending in the application.

2. RCE filed on 1/25/2006 has been received and entered.

3. Applicants' remark has been considered and overcome the prior arts of the record.

Allowable Subject Matter

4. The following is an examiner's statement of reasons for allowance:

Claims 1-22 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination to teach the claimed combination as recited, especially when these limitations are considered within the specific combination with other limitations of the claim. The prior art fails to discloses or suggest transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal and reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal with the logic level transformed to the second voltage level, wherein the bus operates thereafter at the another bus operating bus width and another bus operating frequency (claim 1). Transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal and reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal with the logic level transformed to the second voltage level, wherein the bus operates thereafter at the optimized bus operating bus width and the optimized bus operating frequency (claim12).

The new closest prior art (US 20050093524) discloses in the abstract and paragraphs 0018, 0022, and figures 3-4, a method for CPU power management and bus optimization includes a bus operates at an initial bus bandwidth and an initial bus frequency; settings of the CPU, the Northbridge and the Southbridge are initialized, such that the CPU operates at a CPU operating frequency with a CPU operating voltage with the signal LDTSTOP# is asserted, and a CPU and operating frequency and voltage adjustment is output by the Southbridge to disconnect the CPU and the Northbridge. The asserting of the signal LDTSTOP# also transforms a high level signal LDTSTOP# to a low level signal LDTSTOP#. The LDT bus connected between CPU and the Northbridge is disconnected when the signal LDTSTPO# is asserted. Next, the Southbridge de-asserts the signal LDTSTOP# when the elapsed time value of the timer initialized reaches another predetermined value. Here, the de-asserting of the signal LDTSTOP# transforms a low level signal LDTSTOP# to a high level signal LDTSTOP#. Thus, the LDT bus connected between CPU operates at the time optimized bandwidth and operating frequency reset in BIOS.

Therefore, the prior art fails to disclose the claimed combination as recited in the present application as set forth above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryan Bui whose telephone number is 571-272-2271. The examiner can normally be reached on M-Th from 7am-4pm, and Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRYAN BUI
PRIMARY EXAMINER

BB

3/6/2006